IN THE CLAIMS

1. (Original) An apparatus, comprising:

a phase detector adapted to determine a phase difference between at least two input signals;

a first circuit adapted to generate a control signal based upon the determined phase difference; and

a second circuit adapted to:

receive a first signal;

receive a second signal;

modify the second signal based upon the control signal; and

provide the first signal and the modified second signal as input signals to the phase detector.

2. (Currently Amended) The apparatus of claim 1, wherein the second circuit is adapted to modify the first signal before providing the modified first signal to the phase detector.

3. (Currently Amended) The apparatus of claim 2, wherein the second circuit is adapted to provide the modified first signal and the modified second signal as input signals to the phase detector, and wherein the phase detector is adapted to determine a phase difference between the modified first signal and the modified second signal.

4. (Original) The apparatus of claim 1, wherein the second circuit comprises a fixed delay and an adjustable delay.

5. (Original) The apparatus of claim 4, wherein the fixed delay comprises at least one delay element.

6. (Original) The apparatus of claim 4, wherein the adjustable delay comprises at least two delay elements, at least one of the delay elements in the adjustable delay being selectable based upon the control signal.

7. (Original) The apparatus of claim 1, wherein the phase detector is capable of providing a signal indicative of the determined phase difference to the first circuit.

8. (Currently Amended) The apparatus of claim 7, wherein the signal indicative of the determined phase difference is a binary signal.

9. (Original) The apparatus of claim 8, wherein the control signal is a binary control signal formed using the binary phase difference signal.

10. (Original) The apparatus of claim 1, wherein the first circuit is adapted to provide a signal indicative of a desired clock signal delay based upon the determined phase difference.

11. (Original) The apparatus of claim 1, wherein the first circuit is a majority filter adapted to provide a signal indicative of the desired clock signal delay in response to at least two consecutive determined phase differences in the same direction.

12. (Original) The apparatus of claim 1, wherein the phase detector is at least one of a latch-type detector, an arbiter-type detector, and a counter-type detector.

13. (Original) The apparatus of claim 1, wherein the second circuit comprises a hysteresis adjuster.

14. (Original) A method, comprising:
receiving a clock signal;
receiving a feedback signal formed using the clock signal;

generating a control signal indicative of a phase difference between the clock signal and the feedback signal; and

modifying the feedback signal based upon the control signal.

15. (Original) The method of claim 14, wherein generating the control signal indicative of the phase difference comprises generating the control signal indicating that the clock signal lags the feedback signal.

16. (Original) The method of claim 15, wherein modifying the feedback signal based upon the control signal comprises introducing a delay into the feedback signal in response to the control signal indicating that the clock signal lags the feedback signal.

17. (Original) The method of claim 14, wherein receiving the control signal indicative of the previous phase difference comprises receiving the control signal indicating that the clock signal leads the feedback signal.

18. (Original) The method of claim 17, wherein modifying the feedback signal in response to receiving the control signal comprises reducing a delay in the feedback signal in response to receiving the control signal indicating that the previous clock signal leads the previous feedback signal.

19. (Original) The method of claim 14, further comprising determining a phase difference between the clock signal and the modified feedback signal.

20. (Original) The method of claim 19, further comprising providing a signal indicative of a desired clock signal delay based upon the phase difference between the clock signal and the modified feedback signal.

21. (Original) The method of claim 20, wherein providing the signal indicative of the desired clock signal delay comprises providing the signal indicative of the desired clock signal delay to an adjustable delay.

22. (Original) The method of claim 20, wherein providing the signal indicative of the desired clock signal delay comprises providing the signal indicative of the desired clock signal delay in response to determining at least two consecutive phase differences between the clock signal and modified feedback signal in the same direction.

23. (Original) The method of claim 14, wherein receiving the clock signal comprises modifying the clock signal.

24. (Original) The method of claim 23, wherein generating the control signal comprises generating the control signal indicative of a phase difference between the modified clock signal and the modified feedback signal.

25. (Original) The method of claim 24, further comprising providing a signal indicative of a desired clock signal delay based upon the phase difference between the modified clock signal and the modified feedback signal.

26. (Original) The method of claim 25, wherein providing the signal indicative of the desired clock signal delay comprises providing the signal indicative of the desired clock signal delay to an adjustable delay.

27. (Original) The method of claim 25, wherein providing the signal indicative of the desired clock signal delay comprises providing the signal indicative of the desired clock signal delay in response to determining at least two consecutive phase differences between the modified clock signal and modified feedback signal in the same direction.

28. (Original) An apparatus, comprising:

means for providing a clock signal;

means for providing a feedback signal;

means for providing a control signal indicative of a previous phase difference between the clock signal and the feedback signal; and

means for modifying the feedback signal in response to the control signal.

29. (Original) The apparatus of claim 28, wherein the means for modifying the feedback signal in response to the control signal comprises means for introducing a delay into the feedback signal in response to a control signal indicating that the clock signal lags the feedback signal.

30. (Original) The apparatus of claim 28, wherein the means for modifying the feedback signal in response to receiving the control signal comprises means for reducing a delay in the feedback signal in response to receiving a control signal indicating that the previous clock signal leads the previous feedback signal.

31. (Original) The apparatus of claim 28, further comprising means for providing a signal indicative of a desired delay based upon at least two consecutive phase differences in the same direction.

32. (Original) The apparatus of claim 28, further comprising means for modifying the clock signal.

33. (Original) A delay locked loop, comprising:

an adjustable delay element adapted to receive an input clock signal and provide an output clock signal;

a control logic coupled to the adjustable delay element; and

a phase detector communicatively coupled to the control logic and adapted to determine a phase difference between the input clock signal and the output clock signal, the phase detector comprising:

a hysteresis adjuster adapted to provide a modified output clock signal based upon the output clock signal and a control signal;

a phase detector core adapted to determine a phase difference between the input clock signal and the modified output clock signal; and

a digital filter adapted to provide the control signal to the hysteresis adjuster based upon the phase difference.

34. (Original) The delay locked loop of claim 33, wherein the hysteresis adjuster is further adapted to provide a modified input clock signal based upon the input clock signal.

35. (Original) The delay locked loop of claim 34, wherein the phase detector core is adapted to determine a phase difference between the modified input clock signal and the modified output clock signal.

36. (Original) The delay locked loop of claim 33, wherein the phase detector core is adapted to provide a signal indicative of the determined phase difference to the digital filter.

37. (Original) The delay locked loop of claim 36, wherein the signal indicative of the determined phase difference is a binary signal.

38. (Original) The delay locked loop of claim 33, wherein the digital filter is adapted to provide a signal indicative of a desired clock signal delay based upon the determined phase difference.

39. (Original) The delay locked loop of claim 38, wherein the digital filter is adapted to provide the signal indicative of the desired clock signal delay to the control logic.

40. (Original) The delay locked loop of claim 38, wherein the digital filter is a majority filter adapted to provide the signal indicative of the desired clock signal delay in response to at least two consecutive determined phase differences in the same direction.

41. (Original) The delay locked loop of claim 33, wherein the hysteresis adjuster comprises a fixed delay and an adjustable delay, the fixed delay including at least one delay element and the adjustable delay including at least two delay elements, at least one of the delay elements in the adjustable delay being selectable based upon the control signal.

42. (Original) The delay locked loop of claim 33, wherein the adjustable delay comprises a plurality of delay elements.

43. (Original) The delay locked loop of claim 33, wherein the control logic comprises a shift register.

44. (Original) The delay locked loop of claim 33, further comprising an intrinsic delay.